What is claimed is:

1. A semiconductor device comprising:

a first semiconductor chip having an electrode terminal:

a second semiconductor chip having an electrode terminal:

a bump electrode made of a first metal for joining said first and second semiconductor chips, said bump electrode being provided on at least one of said electrode terminal of said first semiconductor chip and said electrode terminal of said second semiconductor chip; and

an alloy layer formed on a joining portion where said first and second semiconductor chips are joined with each other via said bump electrode, said alloy layer being made of an alloy of said first metal and a second metal,

wherein said second metal is made of such a metal that can melt at a temperature lower than a melting point of said first metal and be alloyed with said first metal.

2. A semiconductor device comprising:

a first semiconductor chip having an electrode terminal:

a second semiconductor chip having an electrode terminal:

a bump electrode made of a first metal for joining said first and second semiconductor chips, said bump electrode being provided on at least one of said electrode terminal of said first semiconductor chip and said electrode terminal

of said second semiconductor chip; and

a third metal layer having a lower melting point than that of said first metal provided on a joining portion where said first and second semiconductor chips are joined with each other via said bump electrode

3. A semiconductor device comprising:

a first semiconductor chip having an electrode terminal:

a second semiconductor chip having an electrode terminal:

a bump electrode made of a first metal for joining said first and second semiconductor chips, said bump electrode being provided on at least one of said electrode terminal of said first semiconductor chip and said electrode terminal of said second semiconductor chip; and

a detachable material portion provided on a joining portion where said first and second semiconductor chips are joined with each other via said bump electrode, said detachable material being made of such a material that said first and second semiconductor chips can be easily separated from each other at a temperature of 280°C to 500°C.

4. The semiconductor device according to claim 1, 2, or 3, wherein said bump electrode is formed on said electrode terminal of each of said first and second semiconductor chips, so that bump electrodes of said first and second semiconductor chips are joined to each other.

5. The semiconductor device according to claim 1, 2,

or 3, wherein said bump electrode is formed on said electrode terminal of one of said first and second semiconductor chips and a metal layer made of said first metal is formed on said electrode terminal of the other of said first and second semiconductor chips, so that said bump electrode and said electrode terminal are joined to each other.

6. The semiconductor device according to any one of claims 1 to 5, wherein a second metal layer made of said second metal or said third metal layer is provided on a right surface and a side surface of said bump electrode made of said first metal, so that said first and second semiconductor chips are joined to each other via said alloy layer or via said third metal layer.

7. The semiconductor device according to any one of claims 1 to 6, said joining portion where said first and second semiconductor chips are joined to each other has such a fillet formed thereon that is made of an alloy layer of said first metal and said second metal or said third metal layer.

8. The semiconductor device according to claim 1, 4, 5, 6, or 7, wherein said first metal is Au and said second metal is Sn, so that said joining portion has an Au-Sn alloy.

9. The semiconductor device according to claim 2, 4, 5, 6, or 7, wherein said third metal is made of an Au-Sn alloy.

10. A semiconductor device comprising:

a first semiconductor chip having an electrode terminal or a wiring;

a second semiconductor chip having an electrode terminal or a wiring; and

a low-melting point metal layer provided on the surface of said wiring of at least one of said first and second semiconductor chips,

wherein said first and second semiconductor chips are electrically interconnected and joined to each other via said low-melting point metal layer so that said electrode terminal or wiring is face to face each other.

11. The semiconductor device according to claim 10, said first and second semiconductor chips are joined to each other with a couple of wirings, and said low-melting point metal layer is provided on a joining portion, further comprising:

a first insulating layer provided as interposed at a gap between said a couple of wirings except at said joining portion.

12. The semiconductor device according to claim 10 or 11, further comprising:

a second insulating layer provided between said wiring and a passivation film on the surface of said semiconductor chip to flatten the surface of said wiring.

13. The semiconductor device according to any one of claims 10 to 12, wherein said wiring is made of an Au, which is provided so as to connect to said electrode terminal via a barrier metal layer, and

wherein said low-melting point metal layer is made of

an Au-Sn alloy.

14. The semiconductor device according to any one of claims 10 to 12, wherein said wiring comprising:

a Cu wiring made of Cu formed simultaneously with said electrode terminal;

a barrier metal layer provided on said Cu wiring; and

an Au wiring provided on said barrier metal layer,

wherein said low-melting point metal layer is made of an Au-Sn alloy and is provided on said Au wire.

15. The semiconductor device according to any one of claims 10 to 13, wherein said wiring is made of Au formed simultaneously with said electrode terminal, and said low-melting point metal layer is made of an Au-Sn alloy.

16. The semiconductor device according to claim 7, 8, 12, 13, 14, or 15, wherein said Au-Sn alloy constituting said joining portion has an Au-rich composition containing at least 65 weight-percent of Au.

17. The semiconductor device according to claim 7, 8, 12, 13, 14, 15, or 16, wherein an Au-Sn alloy layer of said joining portion has a thickness of 0.8μm or more and 5μm or less.

18. The semiconductor device according to any one of claims 1 to 10, further comprising:

an insulating resin layer provided at a gap between said first and second semiconductor chips joined each other to fill the gap, said insulating resin layer having nearly the same elastic modulus as said bump electrode.

19. The semiconductor device according to any one of claims 1 to 10, further comprising:

an insulating resin layer having a thermal shrinkage factor of 5% or less, which is provided at a gap between said first and second semiconductor chips joined each other to fill the gap.

20. The semiconductor device according to any one of claims 1 to 19, wherein a circuit element is formed in a semiconductor layer at said joining portion of at least one of said first and second semiconductor chips.

21. A method for manufacturing a semiconductor device, in which a first semiconductor chip or substrate and a second semiconductor chip are joined to each other with the surfaces thereof on which an electrode terminal or a wiring are formed respectively as facing each other via metals of the surface of said electrode terminal or said wiring, comprising the steps of:

providing at least one of said metals with a low-melting point metal layer having a lower melting point than that of each of said metals; and

melting said low-melting point metal layer or alloying said metals with said low-melting point metal layer to thereby join said first semiconductor chip or substrate and said second semiconductor chip to each other.

22. A method for manufacturing a semiconductor device, in which a first semiconductor chip or substrate and a second semiconductor chip are joined to each other with the surfaces

thereof on which an electrode terminal or a wiring are formed respectively as facing each other via metals of the surface of said electrode terminal or said wiring, comprising the steps of:

providing at least one of said metals with a low-melting point metal layer having a lower melting point than that of each of said metals; and

liquefying said low-melting point metal layer to thereby diffuse said metals provided on the surface of said electrode terminal or said wiring into the liquefied low-melting point metal, by the liquid-phase diffusion method, thus joining said first semiconductor chip or substrate and said second semiconductor chip to each other.

23. The method according to claim 20, wherein said metals are made of Au and said low-melting point metal layer is made of an Au-Sn alloy or Sn, so that said first semiconductor chip or substrate and said second semiconductor chip are superposed one on the other with said electrode terminals or said wirings thereof as facing each other and heated to a temperature at which said Au-Sn alloy or Sn melts, to be self-aligned and joined with each other.

24. The method according to claim 21, 22, or 23, further comprising the steps of:

alloying said metals provided on the surface of said electrode terminal or said wiring of one of said first and second semiconductor chips with said low-melting point metal layer provided on the surface thereof; and

joining to the other of said first and second semiconductor chips or substrate.